

2D MATERIAL DEVICES FOR LOW POWER LOGIC AND MEMORY APPLICATIONS

BY

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THESIS

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ABSTRACT

This thesis investigates low power tunneling field effect transistors (task 1) and low power ferroelectric memory devices (task 2) based on two-dimensional (2D) materials. In the first task, electrical characteristics of mechanically exfoliated n-type Molybdenum Disulfide (MoS_2) and a new p-type material Germanium Selenide (GeSe) were investigated. The pn junctions based on GeSe/MoS_2 heterostructures were fabricated and showed excellent rectifying characteristics, demonstrating for the first time the viability of using GeSe/MoS_2 heterostructures as 2D pn junctions. In the second project, 2D material ferroelectric field effect transistors (FeFETs), with MoS_2 as the channel material and doped Hafnium Oxide (HfO_2) as the ferroelectric gate dielectrics were explored. The electrical characteristics revealed a ferroelectric memory window, and effects associated with ferroelectric materials such as the wake-up effect and polarization fatigue were observed. Future research in both projects can potentially lead to advances of 2D materials in low power logic and memory applications.

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CHAPTER 1: INTRODUCTION

1.1 Device Scaling and Low Power Electronics

Logic and memory devices are the two key types of devices that make up all of our modern electronic systems – logic devices allow computers to perform complex computations and tasks, and memory devices store the huge amount of data that are generated. Portable electronics such as smartphones and tablets are the primary devices for consumer use, and low power consumption is a critical factor for long battery lifetime. As consumer devices make up a huge fraction of the total use of semiconductor devices, research in low-power electronics for logic and memory devices is becoming more significant.

To meet with the growing demands of the consumer market, the size of transistors has been aggressively scaled down to fit more of them onto a single chip, along with reductions in cost and power consumption per chip. However it is becoming more difficult to continue the scaling down process as we approach the 10 nm regime, as we are starting to approach the size of atoms itself and the absolute physical limit. Issues such as increased electrostatic interaction between neighboring cells due to increased proximity, limit of tunnel oxide thickness due to leakage of charge from quantum mechanical tunneling and also limitations in processing techniques especially from lithography start to arise.

In the past few years, the semiconductor industry has developed with exciting innovations for logic and memory devices. There is an apparent paradigm shift from a 2D design to a 3D design. These included examples for logic devices such as conventional planar Field Effect Transistor (FET) to FinFET, and for memory devices examples such as 2D NAND Flash to 3D NAND Flash. However, considering the long term, a more radical approach is required to

preserve Moore's law, and that involves entirely new structures and materials. The focus of this research is on studying how 2D materials can fit into the roadmap of device scaling, and how it provides solutions for (i) **low-power logic devices**, by realizing the feasibility of a 2D-material Tunnel Field Effect Transistor (TFET), and for (ii) **low-power non-volatile memory devices**, by using 2D-materials to realize the Ferroelectric Random Access Memory (FeRAM) device.

1.2 Motivation — Two-Dimensional (2-D) Materials

Since the first isolation of Graphene in 2004 [1], the research community has started to intensely study 2D materials – from semiconductors such as Molybdenum Disulphide (MoS_2) [2] to insulators such as hexagonal Boron Nitride (h-BN) [3], because of their interesting properties and their potential applications in computing, communication and more importantly, to address the problem of device scaling. Scaling theory predicts that transistors with a thin gate-controlled region can be robust against short-channel effects [4]. Two-dimensional materials, being atomically thin, represent the absolute limit in vertical scaling, so it is only natural to include them in the quest of overcoming the device scaling problem. Additionally they naturally form atomically sharp interfaces, without having to deal with atomic diffusion or dangling bonds [5]. Two-dimensional material heterostructures are also unique: different sheets of pristine 2D materials are “stacked” on top of another and bonded together by van-der-Waals-like forces, and there exists a so-called van-der-Waals gap [6]. Therefore they allow for minimal dislocations and trap states. Two-dimensional materials also add a degree of tunability that does not readily exist in bulk materials. It is now very well known that the bandgap E_G of transition metal dichalcogenides

(TMDs) such as MoS_2 and Tungsten Diselenide (WSe_2) can be tuned by varying the thickness of the material [7], [8].

CHAPTER 2: 2D MATERIALS FOR LOGIC APPLICATIONS

2.1 2D Material Electrical Devices

The most important building block for modern logic devices is the Field Effect Transistor (FET). Conventional bulk material Metal Oxide Semiconductor FETs (MOSFETs) are composed of highly doped source-drain regions joined together by a channel, where the current flows. The channel region is electrostatically controlled by a gate, which is situated above the channel region separated by a dielectric layer. The transistor can then switch between “off” (no current flow through the channel) or “on” states (current flowing through the channel) through varying the conductivity of the channel by the electrode gate. The better the control on the channel conductivity by the gate the better the transistor.

In the design of 2D material transistors, the important factors that impact the performance of the transistors include: (i) the intrinsic properties of the material including the mobility, charge density and band-gap of the materials, and (ii) factors extrinsic to the materials such as choice of metal contacts and dielectric integration. For (i), materials with high mobility are essential because they allow for fast switching and high on-state current [9]. To put things into perspective, conventional Silicon-based CMOS transistors have mobilities of up to $500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [10], and additionally for 2D material transistors to be competitive with Si CMOS-based digital logic devices, current ON/OFF ratios of between 1×10^4 and 1×10^7 and bandgaps exceeding 400 meV are desirable [11]. Band-gap is another important property because it determines the ON/OFF ratio. The prime example is Graphene; despite the extraordinarily high intrinsic mobility of Graphene (of at least $200000 \text{ cm}^2/\text{V-s}$ [12]), its lack of a band-gap results in transistors that cannot be turned off. Efforts to engineer a band-gap

in Graphene resulted in degradation in its mobility [13]. This makes it challenging to implement Graphene into applications for digital logic, and this fueled the search for other 2D materials with band-gaps. One of the very first demonstration of the potential of 2D TMDs was the report of the electrical properties of single-layer MoS₂ transistors with ON/OFF ratios of $\sim 10^8$ [14]. Rapid research in many other n-type 2D materials soon followed, such as Molybdenum Diselenide (MoSe₂), Tungsten Diselenide (WSe₂) and Tungsten Disulfide (WS₂) [15], [16], [17].

For (ii), the choice of metal contacts is becoming more significant in transistor design. Recent studies on transistors based on MoS₂, MoSe₂, WS₂ and WSe₂ have shown that the transistors are Schottky barrier controlled and not Ohmic, and in some cases results in high contact resistances [18]. This is because there is the issue of doping in 2D materials (discussed briefly in the next paragraph) that prevents the formation of a metal-highly doped semiconductor interface that is employed to reduce contact resistances in conventional transistors, leading to most 2D transistor designs adopting a metal-intrinsic semiconductor interface. This is an issue for aggressively scaled devices as the desired electrical properties such as steep current turn-on can be masked by the Schottky diode behavior. Additionally, beyond Schottky barrier physics, there are also additional complications such as the metallization of TMDs and fermi-level pinning that disrupts our understanding in the metal-semiconductor interfaces [19]. In some cases, low temperature measurements required to extract certain material properties does not bode well as the current-voltage behavior is completely dominated by the Schottky diode characteristics. The general trend is to use high work function metals for p-type transistors and low-work function metals for n-type

transistors, although this does not always work. For example, it is difficult to achieve low contact resistance in WS_2 using low work function metals because the charge neutrality level is near the middle of the band-gap [20]. Thus research in the electrical contacts to 2D semiconductors is one of the intense areas in the field.

For applications of complimentary devices in CMOS digital logic, both p-type and n-type semiconductors are crucial. While there exists an abundance of research data on n-type 2D materials, the research on p-type 2D materials is less established. One of the reasons is due to the complication of doping in 2D materials. Traditional doping methods using dopant diffusion or ion-implantation commonly used for conventional bulk semiconductors are not suitable for 2D materials due to unavoidable damage during the process. Doping techniques that are being explored include chemical doping by surface modification and electrostatic doping [21].

Another promising approach is to use different 2D materials for n- and p-types. In 2014, few-layer p-type Black Phosphorus (BP) transistors were also demonstrated with very high carrier mobilities ($984 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$) [22]. However it was also reported that BP is unstable in ambient conditions, degrading in the matter of hours, and typically requires passivation of the material in order for the transistor performance to last long. Other p-type based transistors based on MoSe_2 , WSe_2 and Tungsten Disulfide (WS_2) have also been demonstrated [23], [24], [25], but most of the materials are intrinsically doped and in most cases require electrostatic doping. The objective of this study is to investigate a new type of unexplored p-type group-IV monochalcogenide, Germanium Selenide (GeSe), and its potential in future devices.

Bulk group-IV monochalcogenides have been studied in the past because they have many favorable properties that include high stability and high earth abundance [26], [27], however their 2D material counterparts have been relatively unexplored. One of the group-IV compounds that potentially have very useful properties is Germanium Selenide (GeSe). For example, it has been found that GeSe monolayer has a direct band-gap of 1.16 eV [28], very suitable for photovoltaics [29], and has been shown to be a p-type material, adding to the relatively smaller family of available p-type 2D materials. GeSe has giant piezoelectricity [30], has properties (band-gap and effective mass) that can be tunable by application of strain [31], and has a small carrier effective mass, making it very versatile as a semiconductor material with many different potential applications. In our study, we plan to look at GeSe as a potential P-type material to complement other n-type 2D materials.

Additionally, based on a recent theoretical study on Group IV- monochalcogenides [32], GeSe is predicted to have an electron affinity of around 2.6 eV, which is much smaller than the electron affinity in MoS₂ (4.42 eV). Therefore depending on the band-gap of GeSe, the hetero-structure of GeSe/MoS₂ may result in a type II (staggered) or a type III (broken gap) band-alignment. An investigation onto this new monochalcogenide-dichalcogenide hetero-junction is therefore useful for future applications in electronics (e.g. tunnel field effect transistors, described in Section 4.1) and optoelectronics.

2.2 Device Fabrication

The FET characteristics of GeSe and the possibility of GeSe/MoS₂ as a pn hetero-junction diode were investigated. The hetero-structure was fabricated based on the mechanical exfoliation and transfer method. Multilayer GeSe flakes have been mechanically exfoliated from bulk crystals using adhesive tapes [33] onto a SiO₂/p-doped Si substrate.

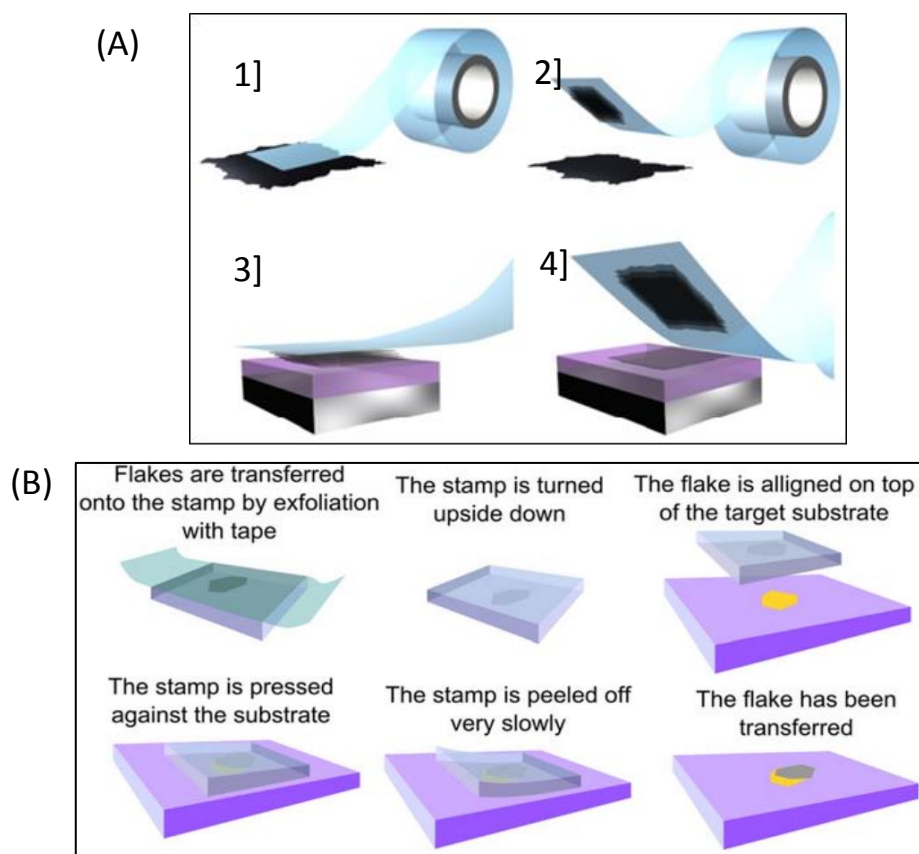


Figure 1: (A) Mechanical exfoliation of 2D material flakes from bulk crystals, and tape transfer onto substrate material. Procedure steps are numbered (1) to (4). Image reproduced from [33]. **(B)** Procedure to align and stack different 2D material flakes to form hetero-structures. Image reproduced from [34].

Then multilayer MoS₂ flakes were transferred onto a viscoelastic stamp supported by a glass slide (following the method from a dry-transfer study [34] Figure 1(B)), aligned using a microscope and transferred onto the GeSe flake via a mechanical micromanipulator stage. This transfer process works on the principle of viscoelasticity of the gel-film and is a clean, dry and efficient process, compared to other wet transfer processes [35], [36].

Figure 2 shows one of the fabricated GeSe/MoS₂ hetero-structure devices, with six metal contacts deposited. The GeSe and MoS₂ hetero-structure flakes were transferred onto a highly p⁺⁺ doped Silicon substrate with 90 nm thick SiO₂. The length and width of the MoS₂ flake is around 30 microns and 7.32 microns, respectively, while the length and width of the GeSe flake is around 25 microns and 6.9 microns, respectively. Six individual metal contacts (M1, M2, M3 for MoS₂ and G1, G2, G3 for GeSe) were then designed by electron-beam lithography and deposited (30 nm Titanium/20 nm Gold) via electron beam evaporation. Because the flakes were long enough, additional contacts were deposited to measure the single material FET characteristics.

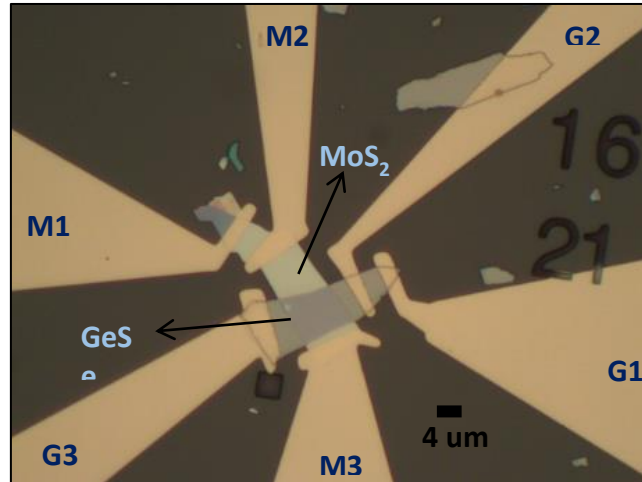


Figure 2: Optical microscope image of a MoS₂ FET, GeSe FET, and MoS₂/GeSe junction device. The GeSe flake lies below the MoS₂ flake, forming a van der Waal's hetero-structure. The scale bar is 4 μm.

2.3 Results and Discussion — Electrical Characteristics

The devices were measured using a Janis Vacuum Probe station and a Keithley 4200 SCS parametric analyzer, under high vacuum conditions (pressure: $\sim 1\text{E-}5$ Torr). This is because the stability of GeSe devices under atmospheric conditions is still unclear; GeSe has a similar structure to BP, and BP is unstable in room temperature. For measuring the individual FETs, the Drain Current-Drain Voltage ($I_D V_D$) and Drain Current-Gate Voltage ($I_D V_G$) characteristics were measured by applying a voltage bias between M1-M2 for MoS₂, and G1-G2 for GeSe, and the gate bias was applied through the highly doped P++ substrate (i.e. via global back-gating).

Figures 3 (A) and (B) shows the $I_D V_D$ and $I_D V_G$ electrical characteristics of the measured MoS₂ FET. The MoS₂ $I_D V_D$ curve shows a linear relationship between the voltage applied and current measured, indicating the contacts are ohmic, and also show very large current values, in the order of $0.1\ \mu\text{A}$ with only a small bias applied ($0.01\ \text{V}$), which is due to the high carrier density in the material. The $I_D V_G$ curve of MoS₂ shows a typical n-channel $I_D V_G$ curve, that is the device turns on with increasingly positive gate bias, with an extracted threshold voltage V_T of $\sim -6.5\ \text{V}$, indicating that the MoS₂ flake is likely highly doped. The field effect mobility was calculated to be around $50\ \text{cm}^2/\text{Vs}$, and an ON/OFF ratio of at least 10^5 was observed. These results are consistent with reported values in literature and show that the exfoliated flakes are of good quality. Figures 4 (A) and (B) show the $I_D V_D$ and $I_D V_G$ electrical characteristics of the measured GeSe FET, respectively. Surprisingly the $I_D V_D$ characteristic of the measured GeSe transistor (and other fabricated GeSe transistors) show some anisotropy in which the negative voltage quadrant shows a linear characteristic, indicating

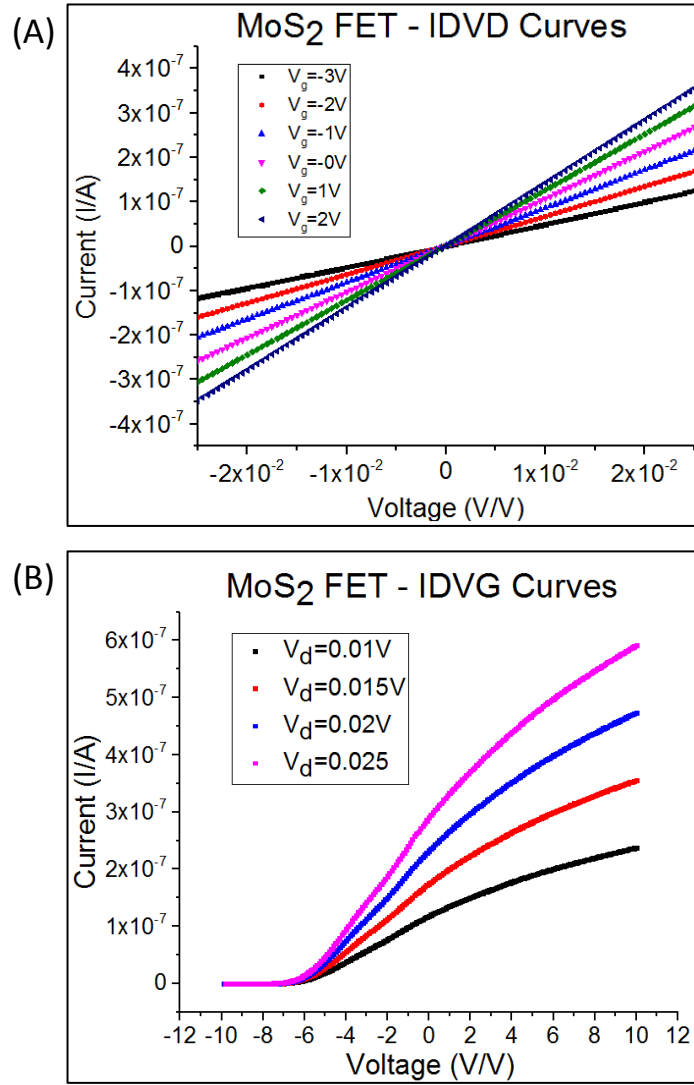


Figure 3: (A) $I_D V_D$ characteristics of individual MoS₂ FET at different gate biases, showing ohmic characteristics. **(B)** $I_D V_G$ curves of MoS₂ FET with different drain biases, showing n-type behavior of MoS₂ FET.

ohmic contacts, but the positive quadrant shows Schottky diode behavior. The GeSe $I_D V_G$ shows a typical p-channel characteristic, which confirms that GeSe is naturally p-doped. Currently there are no literature results on the electrical characteristics of GeSe for comparison with our results. The field-effect mobility extracted from these GeSe FETs are $\sim 1 \text{ cm}^2/\text{V}\cdot\text{s}$. This extraction did not take into account the contact resistance, and the true carrier mobility will most likely be higher. This will be measured in the future via Hall effect measurements.

Figure 4 (C) shows the electrical characteristics of the GeSe/MoS₂ junction, with the source contact on the MoS₂ side and bias applied on the GeSe side. The curve is clearly a pn diode curve, with a current increase exponentially at forward bias, and remains at a very small current at reverse biases. This shows that the GeSe/MoS₂ has rectifying characteristics, and it can be potentially used to build junction field effect transistors and tunneling field effect transistors in future studies.

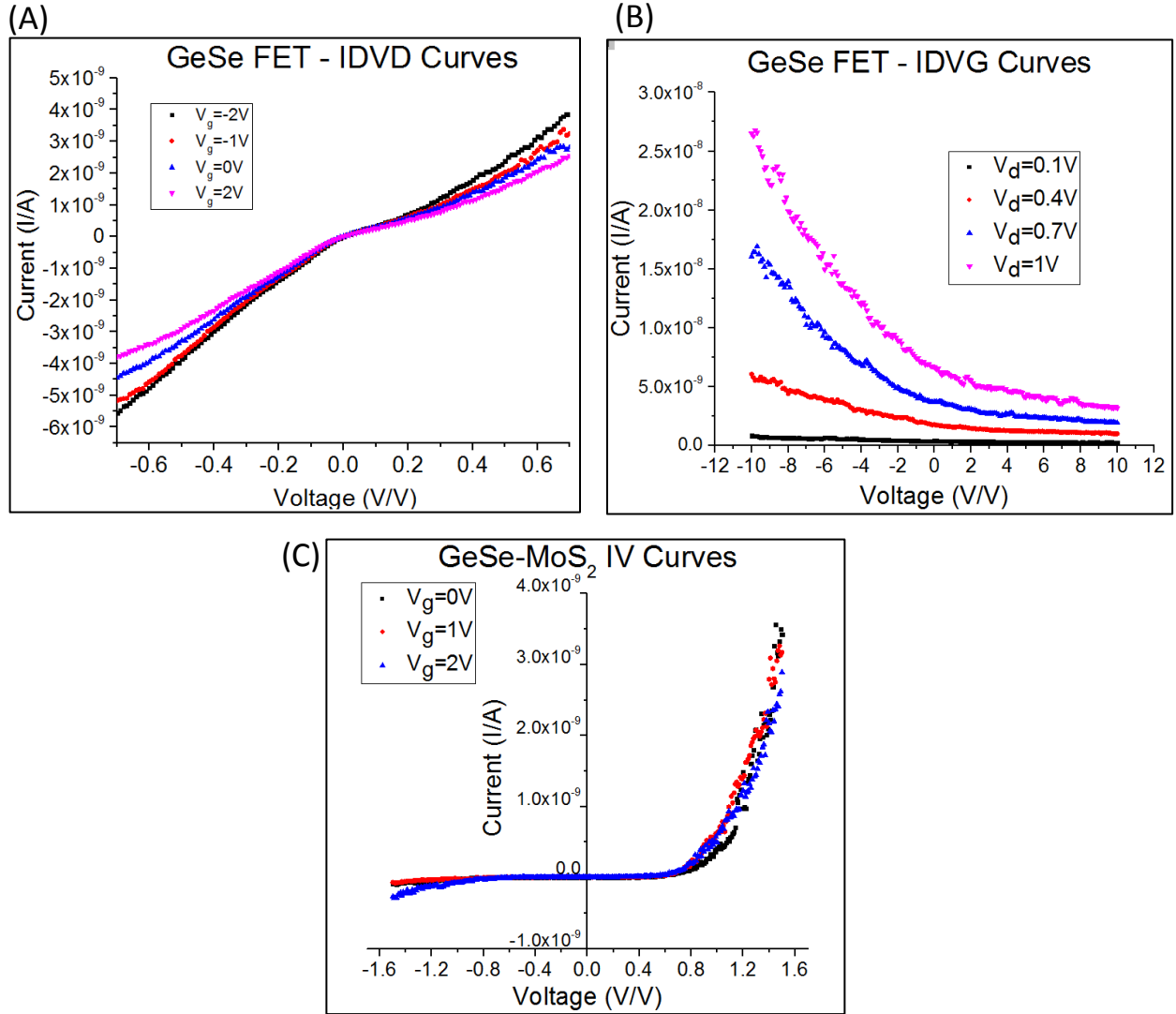


Figure 4: (A) $I_D V_D$ characteristics of individual GeSe FET at different back-gate biases. (B) $I_D V_G$ curves of MoS₂ FET at different drain biases, showing p-type behavior of GeSe FET. (C) I-V characteristics of GeSe/MoS₂ P-N hetero-junction, showing good rectifying behavior.

CHAPTER 3: HAFNIUM OXIDE FERROELECTRICS FOR MEMORY APPLICATIONS

3.1 Introduction — Memory Devices

Since the early 2000s, Solid State Drives (SSDs) have started to slowly but inevitably penetrate the computer market because of their speed, resistance to physical shock, lower latency and higher reliability compared to mechanical Hard Disk Drives (HDDs). As of 2014 most SSDs use NAND-based non-volatile flash memory [37], a type of memory that retains data even without power. The introduction of popular handheld devices such as the iPhone and iPad has caused a surge in demand for flash-based memory. The Non-Volatile Memory (NVM) market is growing exponentially each year, with an estimated demand of 160 billion GBs of memory in 2016, with the greatest growth drivers from personal computer (PC) SSDs, handheld SSDs and enterprise SSDs [37].

The main type of NVM memory is Silicon-based flash memory, and it is based on a floating gate transistor. The structure is made of a MOSFET with an additional floating gate in between the channel and the top gate (Figure 5), which is used to store charges (and hence data) even when the device is turned off. The stored charges alter the threshold voltage V_{TH2} of the device from the original threshold voltage V_{TH1} . Therefore the memory state of the device can be detected by applying a threshold voltage in between V_{TH1} and V_{TH2} , and sensing the output current. The memory state can be programmed by placing charges or erased by removing charges from the floating gate. There are two types of memory: NOR, which has fast access times and fast programming but has a large cell size, and NAND, which has slow access but a much smaller cell size. Therefore it is inevitable that NAND-type memory can

scale down further than NOR-type memory and become the more dominant of the two.

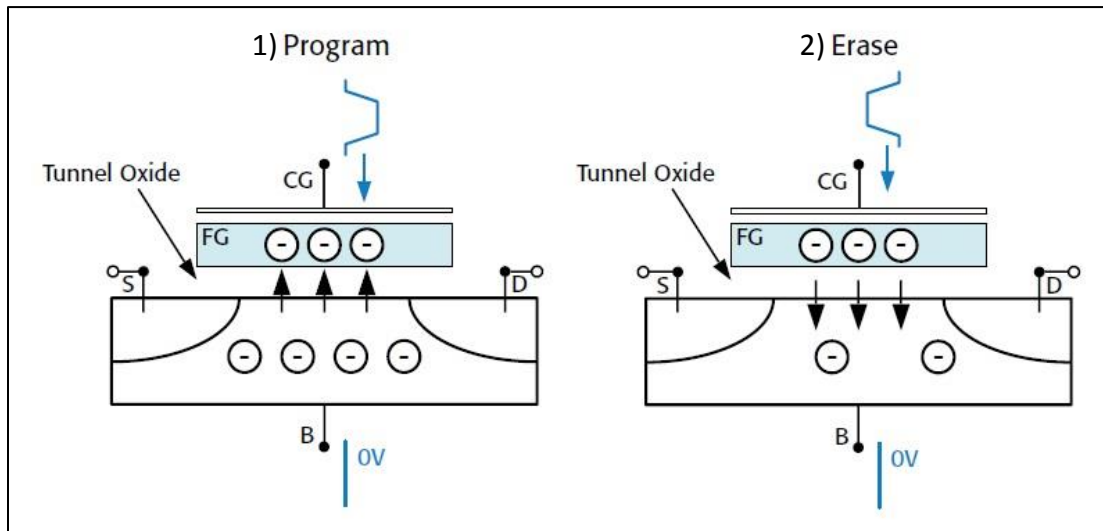


Figure 5: Working process of a floating-gate transistor. During the “Program” phase 1 a large +VE gate voltage is applied, attracting and causing negative charges to tunnel across the tunnel oxide into the floating gate (FG). This shifts the threshold voltage V_{T1} to a higher positive value. Similarly during the “Erase” phase 2, a large -VE gate voltage is applied, repelling and causing negative charges trapped in the floating gate to tunnel out of the floating gate and into the channel. This shifts the threshold voltage to a lower positive value $V_{T2} < V_{T1}$.

To meet with the growing demands of the consumer market and industries, the size of transistors has been aggressively scaled down to fit more of them onto a single chip, along with reductions in cost and power consumption per chip. The node feature size of transistor chips has been scaled down from 130 nm in 2001 to 65 nm in 2006 and is expected to scale down to 10 nm in 2016 [38]. The scaling down of SSD memory has resulted in a drastic drop in cost per GB from USD ~\$260 in 2003 to only USD \$0.28 in 2015 [39]. However it is becoming more difficult to continue scaling down as we approach the 10 nm regime, as we are starting to approach the actual size of atoms themselves and the absolute physical limit. In addition, issues such as increased electrostatic interaction between neighboring cells due

to increased proximity, limit of tunnel oxide thickness due to leakage of charge from quantum mechanical tunneling and also limitations in processing techniques, especially in lithography, start to arise. Most importantly for Flash memory, charge retention becomes an issue: for example, at 20 nm half-pitch, the number of electrons stored in the floating gate is in the order of 100 electrons [40]. If the specifications of flash memory storage dictates < 20% of charge loss in 10 years, that limits the leakage current to < 1 electron/year. Therefore it is imperative that we start to explore new technologies and innovate strategies to overcome the issues of scaling and to preserve Moore's law.

3.2 Ferroelectricity and Ferroelectric Memory Devices

A material is described as ferroelectric when it can exhibit a spontaneous electric polarization state that can be reversed by the application of an external electric field. Unlike dielectric materials, which have a linear relationship between polarization and the applied electric field, ferroelectrics (and paraelectric materials) have a nonlinear polarization vs. electric field relationship. However, the key distinguishing features of ferroelectric materials are (i) existence of remanent polarization, i.e. the material still exhibits polarization even when there is no electric field applied, which, more importantly, leads to (ii) the existence of hysteresis loops, which is the polarization of the material and thus will not only depend on the current electric field applied but also its history, giving rise to "memory loops" (Figure 6). Because of this "memory effect", ferroelectric materials can be considered as candidates for memory devices. In fact this idea is not a new idea at all. Its application in a Ferroelectric RAM (FeRAM) was first proposed in 1963 [41]. However, because of problems in the

depolarization field and finite gate leakage current, the non-volatile FeRAM transistor still has difficulties penetrating the market and so far only remains a relatively small part of the overall semiconductor market.

Despite this, the research in FeRAM has intensified over the past decade, as part of the initiative to seek out alternatives to flash memory. Among the other emerging memory technologies available (phase change RAM, resistive RAM, FeRAM, etc.), FeRAM has the advantage of having among the lowest in both read/write and leakage power. It is also non-volatile and it has a small cell size (almost equivalent to Flash memory) making it highly scalable and suitable for high density memory. The working principles of FeRAM is described in Figure 6. Despite these advantages, state-of-the-art FeRAM based on perovskite material has poor scalability and limited compatibility with industry manufacturing processes (e.g. lead-based materials, oxide electrodes and thermal budget requirements [42], [43]). Only recently, ferroelectricity in Hafnium Oxide (HfO_2) has been discovered when exposed to certain processing conditions. Authors have shown that doping HfO_2 with materials such as Silicon, Aluminum and Zirconium [44], [45], [46] combined with an annealing step can induce a crystalline phase in HfO_2 that has ferroelectric characteristics. HfO_2 has been studied extensively over the past decade and is a well-established high-k dielectric material for memory and logic device applications. Therefore integrating HfO_2 into FeRAM technology, along with 2D materials such as MoS_2 , may yield new perspectives and enormous benefits in scalability and performance.

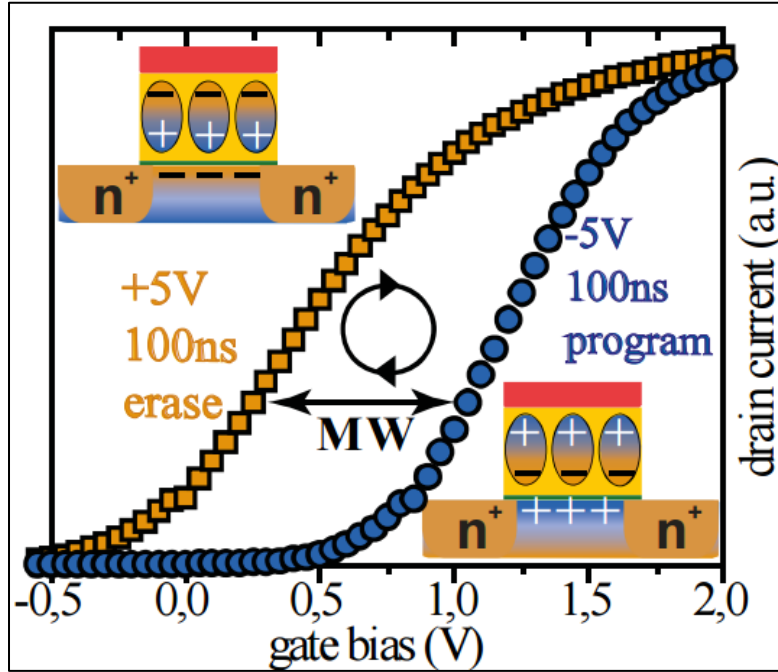


Figure 6: In Ferroelectric FETs, the structure is very similar to a regular MOSFET except that the dielectric material is replaced with the ferroelectric material (yellow region). Memory states are stored based on the polarization state of the ferroelectric material. When the polarization state opposes the direction of the electric field coming from gate bias (bottom right), the threshold voltage V_T will have larger value (blue curve) as a larger bias is required to balance out the opposing polarization states, representing a digital “0” bit/OFF-state. When the states are in the opposite direction (upper left), assisting the gate electric field, V_T will be lower (orange curve), representing a digital “1” bit/ON-state. The different V_T forms a **memory window (MW)** in a double I-V sweep. To set the polarization state, a significantly larger gate bias (in this example, 5V) is applied to induce the polarization states (+VE bias for ON-state, and -VE bias for OFF-state). These voltages are known as WRITE and ERASE voltages. Reproduced from Ref. [44].

3.3 Ferroelectricity in Hafnium Oxide

Ferroelectricity is strongly related to the crystal structure of the material, and only non-centrosymmetric space groups can exhibit piezoelectric and ferroelectric phases. One of the first discovery of ferroelectricity in HfO_2 was HfO_2 thin films doped with Si in 2011 [47], with the discovery of a non-centrosymmetric orthorhombic phase in HfO_2 . Prior to that study HfO_2 was known to exist in three different phases: monoclinic, tetragonal and the cubic phases, and all previously reported HfO_2 bulk are centrosymmetric and non-ferroelectric [48]. HfO_2 is known to be stable in the monoclinic phase at room temperature and only exists in the tetragonal phase at temperatures as high as 2050 K, but (i) the tetragonal phase can be extended to lower temperatures in thin films and (ii) studies showed that presence of top electrode during crystallization of HfO_2 suppresses the monoclinic phase [49], [50]. The use of thin films allows the transformation into the tetragonal phase at a lower temperature e.g. at 1273 K, and the effect of the SiO_2 is to reduce the stability of the monoclinic phase. Boscke et al. furthered the study by investigating the effect of mechanical encapsulation on HfO_2 below the crystallization temperature, i.e. encapsulating amorphous HfO_2 films, and lower Si content, where stabilization of the tetragonal phase is not yet complete. The investigation compared capped and uncapped HfO_2 annealed at 1000 °C for 20 s, which is believed to initiate nucleation in the metastable tetragonal phase, and found that during cooling the mechanical encapsulation forces stress on the HfO_2 and transforms the crystal into an orthorhombic $\text{Pbc}2_1$ phase, instead of the usual monoclinic phase [47].

3.4 Processing and Device Fabrication

Ferroelectric FET (FeFET) devices, with HfO_2 as the ferroelectric gate dielectric and MoS_2 as the channel material, have been fabricated (Figure 7) and measured. The Hafnium ferroelectric layer of interest in this case is situated below the MoS_2 channel. The reason for adopting this inverted structure was to ensure that the MoS_2 can be transferred only after the high temperature annealing process for inducing ferroelectricity in Hafnium Oxide, as it may cause damage to the MoS_2 film. However, this design also has a flaw in that the top electrode may act as a floating gate that allows trapping of charges, which may contribute to a charge-based memory storage effect. This factor was kept in mind when analyzing the measurement results. Future device designs will address this shortcoming.

The process flow for the fabrication of the FeFET is outlined in Figure 8. A 90 nm thick pre-grown SiO_2 on heavily p-doped Si was used as the substrate. Firstly, a global 60 nm thick Titanium (Ti) bottom electrode was deposited using a Cooke electron-beam evaporator. Then 16 nm thick Hafnium Oxide doped with 5.26% Aluminum was deposited using a Cambridge NanoTech Atomic Layer Deposition system, via commercially available metal organic precursors tetrakis (ethylmethylamino)hafnium (TEMAH) and trimethylaluminium (TMA). The percentage of doping was controlled by maintaining a cycle ratio of 18:1 for depositing HfO_2 and Al_2O_3 , respectively, with the total thickness of the film kept at 16 nm. The deposition temperature was relatively lower at 250 °C and 300 °C. A top Ti electrode was then deposited using optical lithography and e-beam evaporation to act as the top mechanical encapsulation layer. The encapsulated amorphous HfO_2 films were then annealed for 30 secs at 1000 °C to crystallize the HfO_2 films. Finally, a 25 nm thick Silicon

Nitride layer was then deposited via a STS mixed-frequency nitride Plasma Enhanced Chemical Vapor Deposition (PECVD) system, applied to prevent contact of the top Ti electrode with the MoS₂ channel.



Figure 7: The final structure of the MoS₂ FeFET based on HfO₂. Notice that this “inverted” structure has the source, drain and channel located above the ferroelectric stack designed to allow the transfer of the CVD grown MoS₂ onto the device only after the 1000 °C annealing process, which may cause damage to the MoS₂.

The next step was to transfer MoS₂ onto the sample, and the method used was a wet Potassium Hydroxide (KOH) etching transfer method suitable for transferring large-scale CVD grown 2D materials. Because of the stable chemical and physical properties of MoS₂, these kinds of common acids (e.g. HCl) and bases (KOH) can be used at room temperature without reaction with MoS₂. A schematic of the transfer process is shown in Figure 9 (A). The single layer CVD-grown MoS₂ was obtained from our collaborators at the National Tsing Hua University (Prof. Yi-Hsien Lee’s group) and was grown on a SiO₂ substrate. A layer of polymethyl methacrylate (PMMA), commonly used as electron-beam lithography resist, was first spun coated at 4000 RPM onto the MoS₂ sample and acts as film support.

The sample was then immersed in a solution of 40% KOH warmed to 60 °C to etch away the SiO₂, leaving the MoS₂ and PMMA floating on the surface. A blank SiO₂/Si substrate was then used to scoop up the floating MoS₂ and PMMA, and was rinsed for several rounds in de-ionized water. The film was finally scooped up with the actual sample and treated with acetone to remove the PMMA support layer.

To complete the FET structure, two more steps were necessary. Since the MoS₂ is a blanket layer covering the whole sample, it is necessary to define channels unique to each device. MoS₂ channel patterns of widths 5 µm were defined by electron-beam lithography and etched via O₂ plasma etching using a Diener Plasma Descum system. Source drain contacts of 30 nm Ti/20 nm Au were then deposited via electron-beam evaporation.

3.5 Results and Discussion

The devices were measured using a Keithley 4200 SCS parametric analyzer. Firstly the $I_D V_G$ electrical characteristics of the regular MoS₂ FETs were measured. Figure 10 shows a regular n-type MoS₂ curve, demonstrating that the MoS₂ FET is functional. As explained in Figure 6, commonly a double I-V sweep (i.e., biasing the gate voltage from a negative value to a positive value then back to a negative value) is performed to observe a ferroelectric window. To differentiate between the mechanisms of (i) charge trapping and (ii) ferroelectricity, the direction of the loop when the double sweep is performed was noted (i.e. clockwise: charge-trapping or counterclockwise: ferroelectricity).

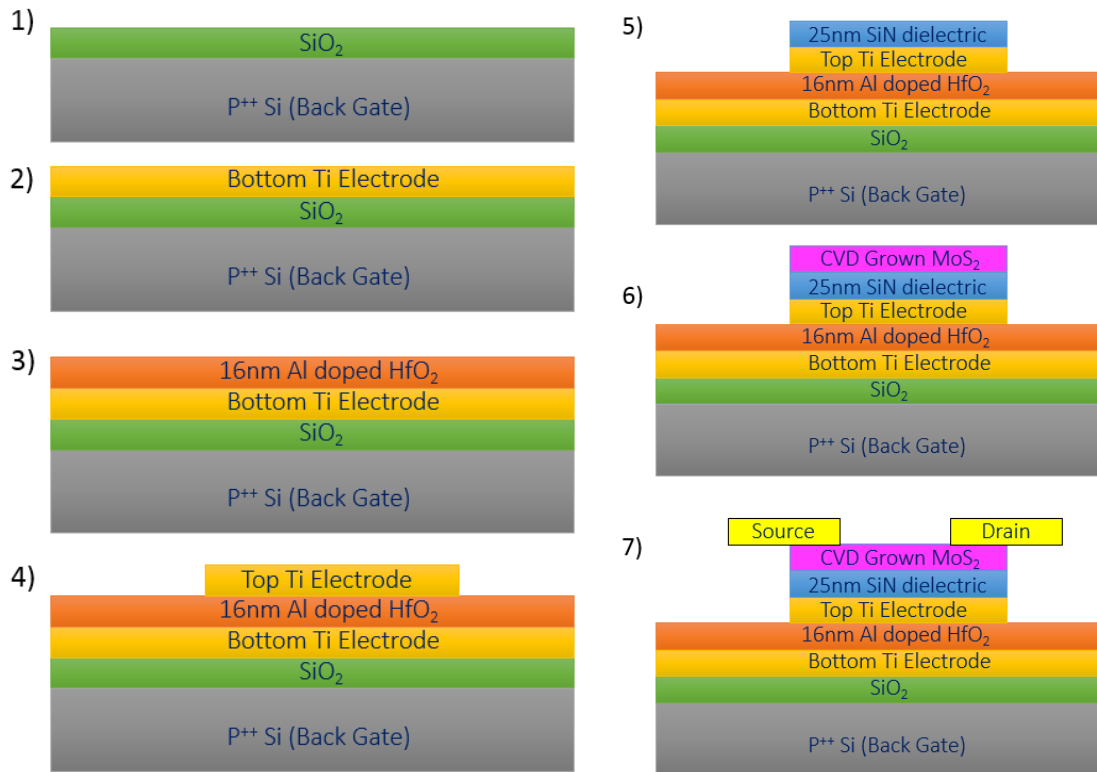
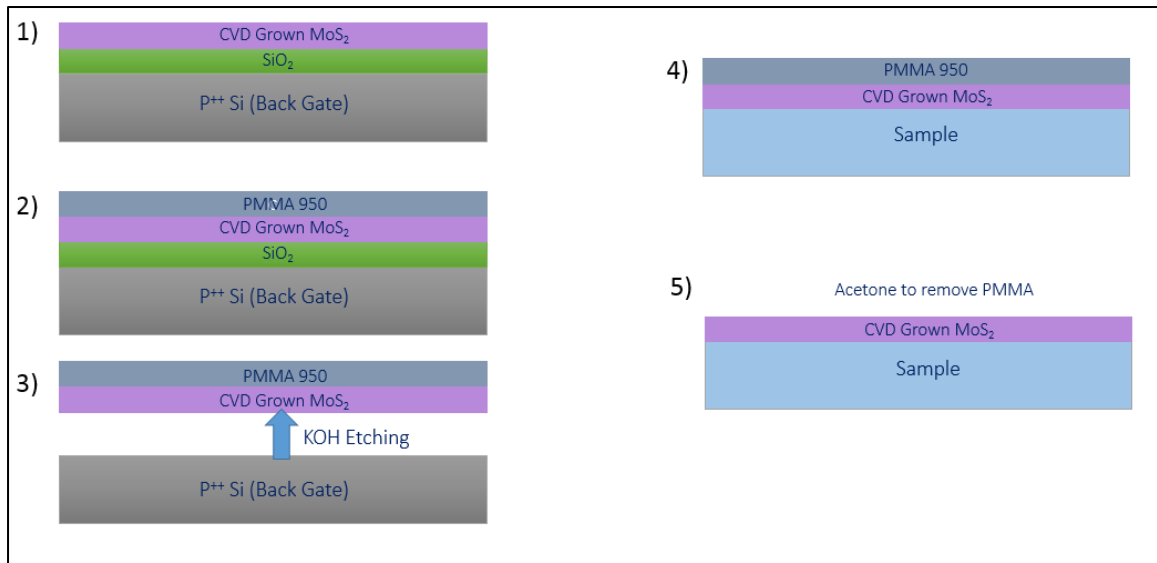


Figure 8: Fabrication process steps of FeFET device. (1) Bare 90 nm SiO_2/Si . (2) Deposition of bottom electrode via e-beam evaporation. (3) Deposition of 16 nm Al-doped HfO_2 via atomic layer deposition and rapid thermal annealing at 1000 °C. (4) Deposition of top electrode via e-beam evaporation. (5) Deposition of 25 nm SiN dielectric via PECVD. (6) Transfer of single-layer CVD grown MoS_2 onto device stack. The transfer process is outlined in Figure 9. (7) Deposition of source-drain contacts via e-beam evaporation.

(A)



(B)

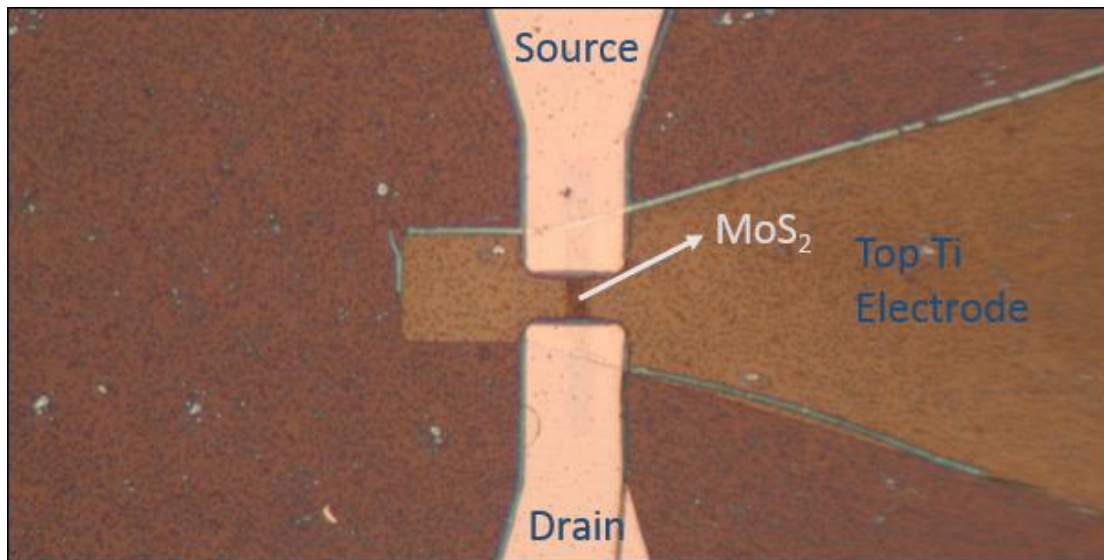


Figure 9: (A) Transfer process steps of MoS₂. (1) Sample with CVD grown MoS₂. (2) Spin PMMA 950 onto MoS₂. (3) Etch away SiO₂ using KOH etchant, leaving the PMMA and MoS₂ film floating. The film is then rinsed several times in DI water. (4) Scoop up film with the device sample. (5) Treat the sample with Acetone to dissolve away the PMMA layer, leaving behind MoS₂ film. **(B)** Optical microscope image of the MoS₂ FeFET structure.

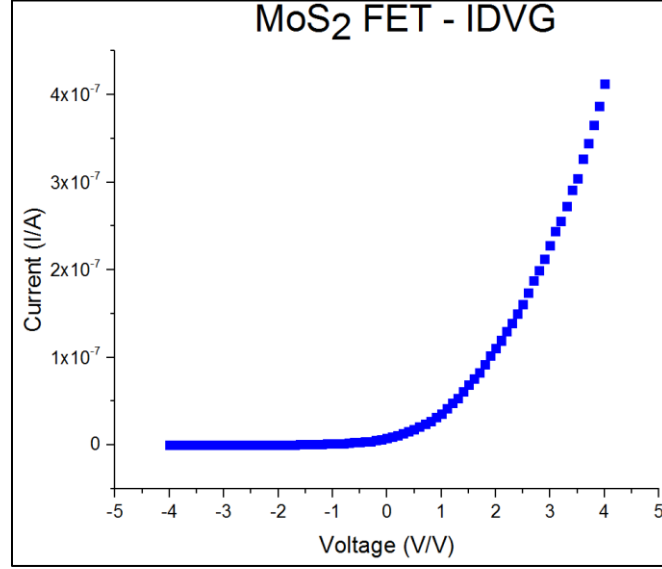


Figure 10: Regular $I_D V_G$ characteristics of MoS₂ FET from MoS₂ FeFET device.

The explanation is as follows: When the sweep starts with a negative voltage and ends with a positive voltage, for (i) negative charges will be attracted to the gate voltage and will tunnel across into the charge trapping layer, and will shift the threshold voltage to a higher value, whereas for (ii), the positive gate voltage induces an opposing polarization state that attracts more inversion charges in the channel, shifting the threshold voltage to a lower value. Therefore, when a reverse sweep is performed, one will observe a counterclockwise loop for ferroelectricity (as V_T is lower) and a clockwise loop for charge trapping (as V_T is higher).

The preliminary results are shown in Figures 11(A) and (B). A ferroelectric memory window was observed (Figure 11), with a counterclockwise loop observed, indicating ferroelectricity instead of charge trapping as the primary mechanism for the observed

hysteresis. The current leakage across the dielectric layer was monitored to ensure there is no significant current tunneling of charge carriers into the floating gate.

The reliability of these memory devices was also tested. Memory devices typically undergo a high number of read-out and write-in cycles during their lifetime. An important requirement criterion for non-volatile memory devices is long-term endurance, i.e. how many read-write cycles it can sustain before it becomes unreliable. For ferroelectric memory devices, this translates to the long-term stability of the switchable polarization states. Two stages of polarization change have been reported for not only conventional PZT materials but also ferroelectric HfO_2 . The first, “wake-up effect”, corresponds to the initial increase in the number of switchable polarization domains, resulting in increases in the ferroelectric memory window. Explanations such as domain wall de-pinning have been attributed to this effect [51]. The second effect, “polarization fatigue”, corresponds to degradation in the polarization states after a high number of switching states [52]. A commonly used procedure in memory endurance testing was used to characterize the devices: a short 5 microsecond negative bias pulse was first applied between the top contact and the bottom contact, to polarize it into the off-state, followed by a 5 microsecond positive bias pulse to polarize it into the on-state; this process constitutes one cycle. The device was then tested under many cycles (up to 20000 cycles) to test its endurance, and then the $I_D V_G$ was measured.

Figures 11 (A) and (B) show the $I_D V_G$ sweeps demonstrating the wake-up effect and fatigue present in the HfO_2 FeFETs, respectively. The plots show sweeps of both polarization states were made after 60, 10000 and 20000 pulse cycles. All of them demonstrated

counterclockwise cycle loops, showing that it is ferroelectric. Figure 11 (A) shows that the width of the memory window “widens” with higher cycles (a blue solid arrow for 60 cycles and an orange dotted arrow for 10000 cycles), demonstrating the wake-up effect.

Additionally, for Figure 11 (B), comparing the current level at the same gate bias voltage for both 10000 (blue, solid arrow) and 20000 (orange, dotted arrow) cycles, it is evident that the current is lower after 20000 cycles for the ON state, demonstrating the fatigue effect.

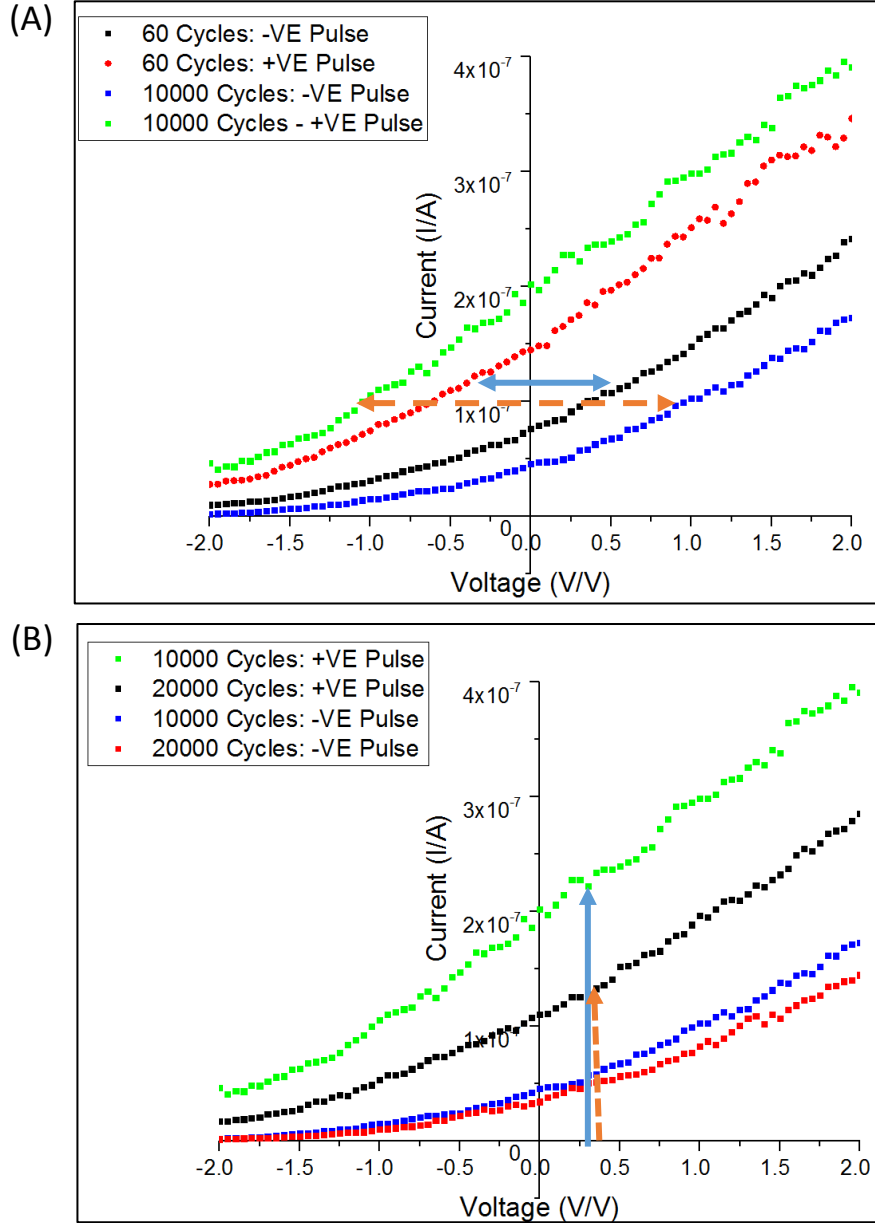


Figure 11: IV measurements of the MoS_2 FeFET after 60, 10000 and 20000 pulse cycles. **(A)** I-V characteristics demonstrating the wake-up effect in the ferroelectric HfO_2 . The width of the memory window after 10000 cycles (orange dotted line) is considerably larger than the width of the memory window after 60 cycles (blue solid line). **(B)** I-V characteristics demonstrating the fatigue effect. The magnitude of the current after 20000 pulsed cycles (orange dotted line) is considerably smaller than the magnitude of the current at 10000 pulsed cycles (blue solid line), which means that the shift in threshold voltage is smaller due to polarization fatigue.

CHAPTER 4: FUTURE WORK

4.1 Tunnel Field Effect Transistors (TFETs)

One of the important metrics in characterizing the performance of a transistor is its Subthreshold Swing (SS, defined as $(\frac{d(\log(I))}{d(V_g)})^{-1}$). A smaller SS is better, as it indicates that only a smaller change in voltage around the threshold voltage is required to turn on the device. The MOSFET has a fundamental lower limit in its SS (60 mV/dec) because it involves the thermionic injection of charge carriers over an energy barrier to turn it on and hence, it is bounded by a thermal limit [53]. This limits the scaling in V_{DD} (the key method in reducing power dissipation in energy efficient devices), as the current leakage during the device off-state would be too large.

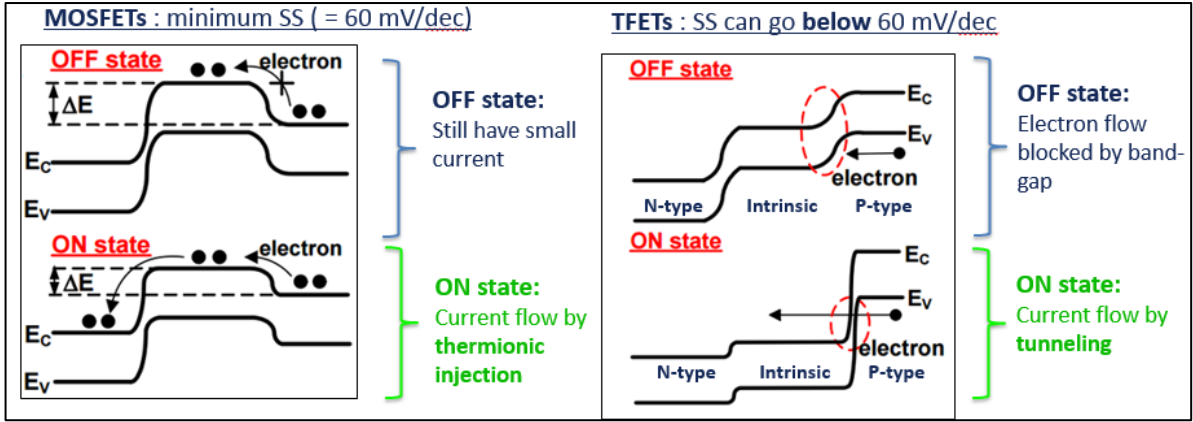
An emerging novel type of device, the Tunnel Field Effect Transistor (TFET) can overcome the voltage scaling limit of MOSFETs by utilizing an entirely different type of process that is independent of the thermal injection process. In TFETs, the carriers in the source are energetically forbidden to tunnel into the channel in the off state, due to the lack of available states in the channel. When the device is turned on (*i.e.*, the conduction band of the channel is below the valence band edge of the source region), the electrons can tunnel from the source into the channel, in a process known as band-to-band-tunneling (BTBT), as illustrated in Figure 12 (A). This novel mechanism allows the SS to be scaled down below 60 mV/dec because the leakage current is completely cut-off by the band-gap during its off-state. There have been reports of sub 60 mV/dec devices made using Silicon, Germanium and III-V based

TFETs [54], [55], [56]. However reports of both large I_{ON} and sub 60 mV/dec SS devices at room temperatures have not been frequently observed [57]. The main challenges with bulk semiconductor TFET devices are the presence of band-tail states and a large number of interface traps, leading to large off-state currents.

To effectively turn on the transistor, the electric field from the gate needs to exercise substantial control over the entire depth of the channel. Therefore the channel needs to be as thin as possible. The 2D materials are perfect for this application over bulk materials, which, with the decrease in thicknesses, introduce problems such as increase in band-gap and surface scattering. Another significant advantage of using 2D materials over bulk materials is the simplicity of vertical TFETs. To maximize the current flow, vertical TFET architectures are preferable because they allow a wider width for current flow. The 2D materials are also advantageous in this respect, because one could simply stack a 2D n-type with a 2D p-type material together to form a vertical TFET.

We are proposing the use of the GeSe/MoS₂ type-II/type-III hetero-junction as a TFET hetero-structure device. Based on preliminary results the hetero-structure showed good promise as a P-N hetero-structure combination, and more studies will be done in investigating the properties of the band-alignment and negative differential resistance phenomena. The proposed device structure is shown in Figure 12 (B).

(A)



(B)

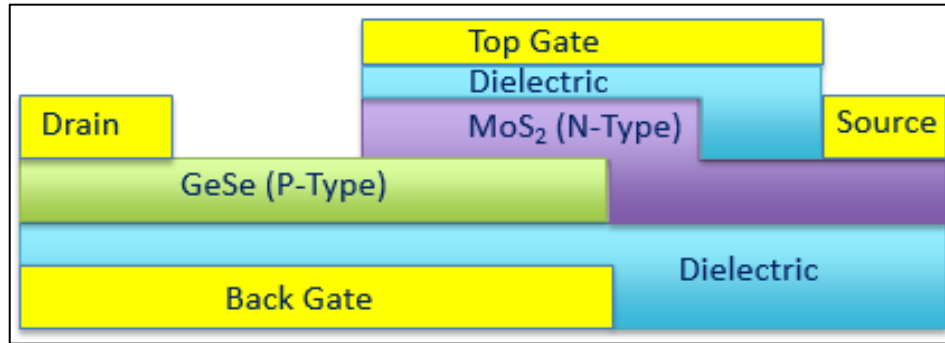


Figure 12: (A) Schematic showing the transistor switching mechanisms in MOSFETs and TFETs. For MOSFETs, the transistor is “barrier-height” controlled, i.e. the transistor either turns off (electron flow blocked by height of channel) or on (electron flow allowed across channel) based on the height of the channel barrier (controlled by gate voltage). However even during the off-state, at finite temperatures some of the electrons still possess enough thermal energy (electrons in the so-called Boltzmann tail) to overcome the energy barrier and flow through. Therefore the on to off switching is not sharp (minimum SS 60 mV/dec). For TFETs, the transistor is “tunnel-barrier” controlled, i.e. electrons will only flow into the channel if there are available states across the tunnel barrier. The difference is, based on the structure of TFETs, that the electrons in the Boltzmann tail are classically forbidden to exist and are effectively cut off by the band-gap, leading to a sharper switching (SS lower than 60 mV/dec possible). Reproduced from Ref. [58] **(B)** Proposed dual-gated hetero-structure device, with each gate locally controlling the electrostatics of MoS₂ and GeSe.

4.2 2D Ferroelectric FETs

Further study will be made on FeFETs based on 2D materials and HfO_2 as a ferroelectric material. In particular, more standard measurements to determine ferroelectricity such as capacitance voltage (C-V) and polarization electric field (PE) measurement techniques will be carried out to monitor the changes in dielectric constant and polarization of the HfO_2 material. The memory retention of the device will also be extensively tested under high temperature conditions and prolonged storage duration. In terms of process conditions, the type of dopant, the relative doping of HfO_2 material, the capping material, different annealing temperatures and duration will be studied to determine the optimal conditions for a wide memory window and low voltage switching. Finally, in terms of channel material, selection of different high mobility 2D materials, such as Black Phosphorus or WSe_2 , will be studied.

REFERENCES

- [1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, *et al.*, “Electric field effect in atomically thin carbon films,” *Science*, vol. 306, pp. 666-669, 2004.
- [2] Y. Yoon, K. Ganapathi, and S. Salahuddin, “How good can monolayer MoS₂ be?” *Nano Letters*, vol. 11, pp. 3768-3773, 2011.
- [3] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, *et al.*, “Boron nitride substrates for high-quality graphene electronics,” *Nature Nanotechnology*, vol. 5, pp. 722-726, 2010.
- [4] F. Schwierz, “Graphene transistors,” *Nature Nanotechnology*, vol. 5, pp. 487-496, 2010.
- [5] H. Fang, C. Battaglia, C. Carraro, S. Nemsak, B. Ozdol, J. S. Kang, *et al.*, “Strong interlayer coupling in van der Waals heterostructures built from single-layer chalcogenides,” *Proceedings of the National Academy of Sciences of the United States of America*, vol. 111, pp. 6198-6202, 2014.
- [6] A. K. Geim and I. V. Grigorieva, “Van der Waals heterostructures,” *Nature*, vol. 499, pp. 419-425, 2013.
- [7] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. Heinz, “Atomically thin MoS₂: A new direct-gap semiconductor,” *Physical Review Letters*, vol. 105, p. 136805, 2010.
- [8] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, “Electronics and optoelectronics of two-dimensional transition metal dichalcogenides,” *Nature Nanotechnology*, vol. 7, pp. 699-712, 2012.
- [9] D. Lembke, S. Bertolazzi, and A. Kis, “Single-layer MoS₂ electronics,” *Accounts of Chemical Research*, vol. 48, pp. 100-110, 2015.
- [10] F. Schwierz, J. Pezoldt, and R. Granzner, “Two-dimensional materials and their prospects in transistors electronics,” *Nanoscale*, vol. 7, pp. 8261-8283, 2015.

- [11] F. Schwierz, "Graphene transistors," *Nature Nanotechnology*, vol. 5, pp. 487-496, 2010.
- [12] B. Radisavljevic, M. B. Whitwick, and A. Kis, "Integrated circuits and logic operations based on single-layer MoS₂," *ACS Nano*, vol. 5, pp. 9934-9938, 2011.
- [13] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science*, vol. 319, pp. 1229-1232, 2008.
- [14] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS₂ transistors," *Nature Nanotechnology*, vol. 6, pp. 147-150, 2011.
- [15] S. Larentis, B. Fallahazad, and E. Tutuc, "Field-effect transistors and intrinsic mobility in ultra-thin MoSe₂ layers," *Applied Physics Letters*, vol. 101, p. 223104, 2012.
- [16] A. Allain and A. Kis, "Electron and hole mobilities in single layer WSe₂," *ACS Nano*, vol. 8, pp. 7180-7185, 2014.
- [17] D. Ovchinnikov, A. Allain, Y-S. Huang, D. Dumcenco, and A. Kis, "Electrical transport properties of single-layer WS₂," *ACS Nano*, vol. 8, pp. 8174-8181, 2014.
- [18] A. Allain, J. Kang, K. Banerjee, and A. Kis, "Electrical contacts to two-dimensional semiconductors," *Nature Materials*, vol. 14, pp. 1195-1205, 2015.
- [19] D. Liu, Y. Guo, L. Fang, and J. Robertson, "Sulfur vacancies in monolayer MoS₂ and its electrical contacts," *Applied Physics Letters*, vol. 103, pp. 183113, 2013.
- [20] J. Kang, S. Tongay, J. Zhou, J. Li, and J. Wu, "Band offsets and heterostructures of two-dimensional semiconductors," *Applied Physics Letters*, vol. 103, p. 012111, 2013.
- [21] G. R. Bhimanapati, Z. Lin, V. Meunier, Y. Jung, J. Cha, S. Das, *et al.*, "Recent advances in two-dimensional materials beyond graphene," *ACS Nano*, vol. 9, pp. 11509-11539, 2015.
- [22] L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, *et al.*, "Black phosphorus field-effect transistors," *Nature Nanotechnology*, vol. 9, pp. 372-377, 2014.
- [23] S. Larentis, B. Fallahazad, and E. Tutuc *et al.*, "Field-effect transistors and intrinsic mobility in ultra-thin MoSe₂ layers," *Applied Physics Letters*, vol. 101, p. 223104, 2012.
- [24] A. Allain and A. Kis, "Electron and hole mobilities in single layer WSe₂," *ACS Nano*, vol. 8, pp. 7180-7185, 2014.

- [25] D. Ovchinnikov, A. Allain, Y-S. Huang, D. Dumcenco, and A. Kis, "Electrical transport properties of single-layer WS₂," *ACS Nano*, vol. 8, pp. 8174-8181, 2014.
- [26] G. A. Tritsarlis, B. D. Malone, and E. Kaxiras, "Optoelectronic properties of single-layer, double-layer, and bulk tin sulfide: A theoretical study," *Journal of Applied Physics*, vol. 113, p. 233507, 2013.
- [27] L. Li, Z. Chen, Y. Hu, X. Wang, T. Zhang, W. Chen, *et al.*, "Single-layer single-crystalline SnSe nanosheets," *Journal of the American Chemical Society*, vol. 135, pp. 1213-1216, 2013.
- [28] G. Shi and E. Kioupakis, "Anisotropic spin transport and strong visible-light absorbance in few-layer SnSe and GeSe," *Nano Letters*, vol. 15, pp. 6926-6931, 2015.
- [29] Y. Hu, S. Zhang, S. Sun, M. Xie, B. Cai, and H. Zeng, "GeSe monolayer semiconductor with tunable direct band gap and small carrier effective mass," *Applied Physics Letters*, vol. 107, p. 122107, 2015.
- [30] R. Fei, W. Li, J. Li, L. Yang, "Giant piezoelectricity of monolayer group IV monochalcogenides: SnSe, SnS, GeSe, and GeS," *Applied Physics Letters*, vol. 107, p. 173104, 2015.
- [31] M. Wu and X. C. Zeng, "Intrinsic ferroelasticity and/or multiferroicity in two-dimensional phosphorene and phosphorene analogues," *Nano Letters*, vol. 16, pp. 3236-3241, 2016.
- [32] A. K. Singh and R. G. Hennig, "Computational prediction of two-dimensional group-IV mono-chalcogenides," *Applied Physics Letters*, vol. 105, p. 042103, 2014.
- [33] K. S. Novoselov and A. H. Castro Neto, "Two-dimensional crystals-based heterostructures: Materials with tailored properties," *Physics Scripta*, vol. 2012, p. 014006, 2012.
- [34] A. Castellanos-Gomez, M. Buscema, R. Molenaar, V. Singh, L. Janssen, H. S. J. van der Zant, *et al.*, "Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping," *2D Materials*, vol. 1, p. 011002, 2014.
- [35] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, *et al.*, "Boron nitride substrates for high-quality graphene electronics," *Nature Nanotechnology*, vol. 5, pp. 722-726, 2010.

- [36] G. F. Schneider, V. E. Calado, H. Zandbergen, L. M. Vandersypen, and C. Dekker, *et al.*, "Wedging transfer of nanostructures," *Nano Letters*, vol. 10, pp. 1912-1916, 2010.
- [37] D. Wouters, "Resistive switching materials and devices for future memory applications," presented at 43rd IEEE Semiconductor Interface Specialists Conference, San Diego, USA, 2012.
- [38] R. C. Johnson. (2008, Jul.). MIT: Optical lithography good to 12 nanometers. EE Times. [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1168971
- [39] Z. Kerekes. (2016, May.). Charting the Rise of the Solid State Disk Market. StorageSearch.com, England. [Online]. Available: StorageSearch.com/chartingtheriseofssds.html
- [40] K. Prall, "Scaling non-volatile memory below 30nm," *IEEE Non-Volatile Semiconductor Memory Workshop*, pp. 5-10, 2007.
- [41] J. L. Moll and Y. Tarui, "A new solid state memory resistor," *IEEE Transactions on Electron Devices*, vol. 10, p. 338, 1963.
- [42] B-D. Hahn, K-H. Kim, D-S. Park, J-J. Choi, J. Ryu, W-H. Yoon, *et al.*, "Fabrication of lead zirconate titanate thick films using a powder containing organic residue," *Japanese Journal of Applied Physics*, vol. 47, p. 5545, 2008.
- [43] K. Kim, "Future memory technology: Challenges and opportunities," *International Symposium on VLSI technology, Systems and Applications*, pp. 5-9, 2008.
- [44] J. Muller, T. S. Boscke, S. Muller, E. Yurchuk, P. Polakowski, J. Paul, *et al.*, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," *IEEE International Electron Devices Meeting*, pp. 10.8.1–10.8.4, 2013.
- [45] S. Muller, J. Muller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, *et al.*, "Incipient ferroelectricity in Al-doped HfO₂ thin films," *Advanced Functional Materials*, vol. 22, pp. 2412-2417, 2012.
- [46] J. Muller, T. S. Boscke, U. Schroder, S. Mueller, D. Braushaus, U. Bottger, *et al.*, "Ferroelectricity in simple binary ZrO₂ and HfO₂" *Nano Letters*, vol. 12, pp 4318–4323, 2012.

- [47] T. S. Boscke, J. Muller, D. Braushaus, U. Schroder, and U. Bottger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, vol. 99, p. 102903, 2011.
- [48] J. Wang, H. P. Li, and R. Stevens, "Hafnia and hafnia-toughened ceramics," *Journal of Materials Science*, vol. 27, pp. 5397-5430, 1992.
- [49] T. S. Boscke, P. Y. Hung, P. D. Kirsch, M. A. Quevedo-Lopez, and R. Ramirez-Bon, "Increasing permittivity in HfZrO thin films by surface manipulation," *Applied Physics Letters*, vol. 95, p. 052904, 2009.
- [50] D. H. Triyoso, P. J. Tobin, B. E. White Jr., R. Gregory, and X. D. Wang, "Impact of film properties of atomic layer deposited HfO₂ resulting from annealing with a TiN capping layer," *Applied Physics Letters*, vol. 89, p. 132903, 2006.
- [51] D. Zhou, J. Xu, Q. Li, Y. Guan, F. Cao, X. Dong, *et al.*, "Wake-up effects in Si-doped hafnium oxide ferroelectric thin films," *Applied Physics Letters*, vol. 103, p. 192904, 2013.
- [52] T. Schenk, U. Schroeder, M. Pesic, M. Popovici, Y. V. Pershin, and T. Mikolajick, "Electric field cycling behavior of ferroelectric hafnium oxide," *ACS Applied Material Interfaces*, vol. 6, pp. 19744-19751, 2014.
- [53] S. M. Sze, *Physics of Semiconductor Devices*, Wiley Interscience, 1981.
- [54] R. Gandhi, Z. Chen, N. Singh, and K. Banerjee, "CMOS-compatible vertical-silicon-nanowire gate-all-around p-type tunneling FETs with < 50-mV/decade subthreshold swing," *IEEE Electron Device Letters*, vol. 32, pp. 1504-1506, 2011.
- [55] F. Mayer, C. le. Royer, J. F-. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, *et al.*, "Impact of SOI, Si_{1-x}Ge_xOI and GeOI substrates on CMOS compatible tunnel FET performance," *IEEE International Electron Devices Meeting*, pp. 1-5, 2008.
- [56] B. Ganjipour, J. Wallentin, M. T. Borgstrom, L. Samuelson, and C. Thelander, "Tunnel field-effect transistors based on InP-GaAs heterostructure nanowires," *ACS Nano*, vol. 6, pp. 3109-3113, 2012.
- [57] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, *et al.*, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, pp. 91-95, 2015.